CLAIMS

What is claimed is:

1. A circuit comprising:

a current source for generating a reference current; and

a frequency doubler circuit coupled to said current source and receiving a first frequency signal and also receiving said reference current, said frequency doubler circuit generating a second frequency signal and using said reference current to compensate for process variation of capacitance and using said reference current to maintain a known duty cycle.

2. A circuit as recited in Claim 1 wherein the value of said second frequency signal is substantially twice the value of said first frequency signal.

3. A circuit as recited in Claim 1 further comprising a control loop circuit for generating an output current, said output current operating in conjunction with said reference current to compensate for process variation of capacitance and using said reference current to maintain a known duty cycle.

4. A circuit as recited in Claim 1 wherein said current source comprises trimmable current control.

5. A circuit as recited in Claim 4 wherein said trimmable current control comprises a plurality of trimmable components.

6. A circuit as recited in Claim 1 wherein said current source is a digital to analog converter circuit.

7. A circuit as recited in Claim 6 wherein said digital to analog converter circuit comprises a trimmable current control.

8. A circuit as recited in Claim 7 wherein said trimmable current control comprises a plurality of trimmable components.

9. A circuit as recited in Claim 6 wherein said digital to analog converter circuit is for generating an oscillator current used in an oscillator circuit, said oscillator circuit for generating said first frequency signal.

10. A circuit as recited in Claim 9 wherein the value of said oscillator current is equal in value to the value of said reference current.

11. A circuit as recited in Claim 5 wherein said plurality of trimmable components are digitally controlled.

12. A circuit as recited in Claim 8 wherein said plurality of trimmable components are digitally controlled.

13. A circuit comprising:

an oscillator circuit for generating a first frequency signal;

a current source for generating a reference current; and

a frequency doubler circuit coupled to said current source and receiving a first frequency signal and also receiving said reference current, said frequency doubler circuit generating a second frequency signal and using said reference current to compensate for process variation of capacitance and using said reference current to maintain a known duty cycle.

14. A circuit as recited in Claim 13 wherein the value of said second frequency signal is substantially twice the value of said first frequency signal.

15. A circuit as recited in Claim 13 further comprising a control loop circuit for generating an output current, said output current operating in conjunction with said reference current to compensate for process variation of capacitance and using said reference current to maintain a known duty cycle.

16. A circuit as recited in Claim 13 wherein said current source comprises trimmable current control.

17. A circuit as recited in Claim 16 wherein said trimmable current control comprises a plurality of trimmable components.

18. A circuit as recited in Claim 13 wherein said current source is a digital to analog converter circuit.

19. A circuit as recited in Claim 18 wherein said digital to analog converter circuit comprises a trimmable current control.

20. A circuit as recited in Claim 19 wherein said trimmable current control comprises a plurality of trimmable components.

21. A circuit as recited in Claim 18 wherein said digital to analog converter circuit is for generating an oscillator current used in said oscillator circuit for generating said first frequency signal.

22. A circuit as recited in Claim 21 wherein the value of said oscillator current is equal in value to the value of said reference current.

23. A circuit as recited in Claim 17 wherein said plurality of trimmable components are digitally controlled.

24. A circuit as recited in Claim 20 wherein said plurality of trimmable components are digitally controlled.

25. A microcontroller comprising:

a bus;

a processor coupled to said bus;

a memory unit coupled to said bus;

an oscillator circuit for generating a first frequency signal;

a current source for generating a reference current; and

a frequency doubler circuit coupled to said current source and receiving a first frequency signal and also receiving said reference current, said frequency doubler circuit generating a second frequency signal and using said reference current to compensate for process variation of capacitance and using said reference current to maintain a known duty cycle.

26. A microcontroller as recited in Claim 25 wherein the value of said second frequency signal is substantially twice the value of said first frequency signal.

27. A microcontroller as recited in Claim 25 further comprising a control loop circuit for generating an output current, said output current operating in conjunction with said reference current to compensate for process

variation of capacitance and using said reference current to maintain a known duty cycle.

28. A microcontroller as recited in Claim 25 wherein said current source comprises trimmable current control.

29. A microcontroller as recited in Claim 27 wherein said trimmable current control comprises a plurality of trimmable components.

30. A microcontroller as recited in Claim 25 wherein said current source is a digital to analog converter circuit.

31. A microcontroller as recited in Claim 30 wherein said digital to analog converter circuit comprises a trimmable current control.

32. A microcontroller as recited in Claim 31 wherein said trimmable current control comprises a plurality of trimmable components.

33. A microcontroller as recited in Claim 30 wherein said digital to analog converter circuit is for generating an oscillator current used in said oscillator circuit for generating said first frequency signal.

34. A microcontroller as recited in Claim 33 wherein the value of said oscillator current is equal in value to the value of said reference current.

35. A microcontroller as recited in Claim 29 wherein said plurality of trimmable components are digitally controlled.

36. A microcontroller as recited in Claim 32 wherein said plurality of trimmable components are digitally controlled.